邏輯設計 Hw#5
Answer
1. Design a combinational circuit that forms the 2-bit binary sum $S_1S_0$ of two 2-bit number $A_1A_0$ and $B_1B_0$ and has both a carry input $C_0$ and carry output $C_2$. Design the entire circuit implementing each of the three outputs with a two-level circuit plus inverters for the input variables. Begin the design with the following equations for each of the two bits of the adder:

\[
S_i = A_i'B_i'C_i + A_i'B_iC_i' + A_iB_i'C_i' + A_iB_iC_i
\]
\[
C_{i+1} = A_iB_i + A_iC_i + B_iC_i
\]

<Ans>

就是把要求的 outputs, $S_1$, $S_0$, $C_2$ 下到用 inputs $A_1$, $A_0$, $B_1$, $B_0$, $C_0$ 表示

\[
C_1 = A_0B_0 + A_0C_0 + B_0C_0
\]

\[
S_0 = A_0'B_0'C_0 + A_0'B_0C_0' + A_0B_0'C_0' + A_0B_0C_0
\]
\[
S_1 = A_1'B_1'C_1 + A_1'B_1C_1' + A_1B_1'C_1' + A_1B_1C_1
\]
\[
= A_1'B_1'(A_0B_0 + A_0C_0 + B_0C_0) + A_1'B_1(A_0B_0 + A_0C_0 + B_0C_0)'+ A_1B_1'(A_0B_0 + A_0C_0 + B_0C_0)' + A_1B_1(A_0B_0 + A_0C_0 + B_0C_0)
\]
\[
= A_1'B_1'A_0B_0 + A_1'B_1'A_0C_0 + A_1'B_1'B_0C_0 + A_1'B_1'A_0'B_0' + A_1'B_1'A_0'C_0' + A_1'B_1'B_0'C_0' + A_1B_1'A_0'B_0 + A_1B_1'A_0C_0 + A_1B_1'B_0C_0
\]

\[
C_2 = A_1B_1 + A_1C_1 + B_1C_1
\]
\[
= A_1B_1 + A_1(A_0B_0 + A_0C_0 + B_0C_0) + B_1(A_0B_0 + A_0C_0 + B_0C_0)
\]
\[
= A_1B_1 + A_1A_0B_0 + A_1A_0C_0 + A_1B_0C_0 + B_1A_0B_0 + B_1A_0C_0 + B_1B_0C_0
\]
2. The following binary numbers have a sign in the leftmost position and, if negative, are in 2’s complement form. Perform the indicated arithmetic operations and verify the answers.
(a) $100111 + 111001$  
(b) $110001 - 010010$

Indicate if overflow occurs for each computation.

<Ans>

(a) $100111 + 111001 = 111111$

\[\begin{array}{c}
111111 \\
100111 \quad (-25) \\
+111001 \quad (+7) \\
\hline
1100000 \quad (-32) \\
\Rightarrow 1000000 \quad (-32) \text{ verified}
\end{array}\]

∴ MSB's carry in = carry out
∴ 無 overflow

(b) $110001 - 010010 = +101110$

\[\begin{array}{c}
110001 \quad (-15) \\
+101110 \quad (+18) \\
\hline
1011110 \quad (-33) \\
\Rightarrow 011111 \quad +31 \text{ verified}
\end{array}\]

∴ MSB's carry in ≠ carry out
∴ overflow发生，所以兩個負數相加竟得到正數
3. Use contraction beginning with an 8-bit adder-subtractor without carry out to design an 8-bit circuit without carry out that increments its input by 00000010 for input $S = 0$ and decrements its input by 00000010 for input $S = 1$. Perform the design by designing the distinct 1-bit cells needed and indicating the type of cell use in each of the eight bit positions.

<Ans>

當$S = 0$，就是加00000010；當$S = 1$，是減00000010，也就是加11111110把 00000010, 11111110當作 $B_7$～$B_0$。

$B_0 = 0, C_0 = 0 \implies S_0 = A_0 \oplus 0 \oplus 0 = A_0$

$\implies C_1 = A_0B_0 + A_0C_0 + B_0C_0 = 0$

$B_1 = 1, C_1 = 0 \implies S_1 = A_1 \oplus 1 \oplus 0 = A_1'$

$\implies C_2 = A_1B_1 + A_1C_1 + B_1C_1 = A_1$

(接下來就沒法化簡了，因為$B_2$～$B_7$可能是0也可能是1)

$S_0$直接拉線，$S_1$接個inverter，$S_2$～$6$是用Full Adders產生，
而最左邊的bit免算$C_{out}$所以用3-input XOR得到$S_7$。
4. Design a combinational circuit that compares two 4-bit unsigned numbers \( A \) and \( B \) to see whether \( B \) is greater than \( A \). The circuit has one output \( X \), so that \( X = 1 \) if \( A < B \) and \( X = 0 \) if \( A \geq B \).

\[
A < B, \text{发生在某一位 } A_i = 0, B_i = 1, \text{而更高位都相等}(A_j = B_j, \text{for all } j > i)
\]
\[
\therefore X = A_3'B_3 + (A_3B_3 + A_3'B_3')A_2'B_2 + (A_3B_3 + A_3'B_3')(A_2B_2 + A_2'B_2')A_1'B_1 + (A_3B_3 + A_3'B_3')(A_2B_2 + A_2'B_2')(A_1B_1 + A_1'B_1')A_0'B_0
\]
不經簡化的電路圖如下(不畫沒關係):

![Diagram](image-url)
5. Design a binary multiplier that multiplies two 3-bit unsigned numbers. Use AND gates and binary adders.

\[ \begin{array}{cccc}
   a_2 & a_1 & a_0 \\
   b_2 & b_1 & b_0 \\
   \times & & & \\
   \hline
   a_2b_0 & a_1b_0 & a_0b_0 \\
   a_2b_1 & a_1b_1 & a_0b_1 \\
   + & a_2b_2 & a_1b_2 & a_0b_2 \\
   \hline
   P_5 & P_4 & P_3 & P_2 & P_1 & P_0
\end{array} \]
6. Design a circuit that multiplies a 4-bit multiplicand (被乘數) by the constant 1010 by applying contraction to the solution to Problem 5.

\[
\begin{array}{cccc}
\text{a}_3 & \text{a}_2 & \text{a}_1 & \text{a}_0 \\
\times) & 1 & 0 & 1 & 0 \\
\hline
\text{a}_3 & \text{a}_2 & \text{a}_1 & \text{a}_0 \\
0 & 0 & 0 & 0 \\
+) & \text{a}_3 & \text{a}_2 & \text{a}_1 & \text{a}_0 \\
\hline
\text{P}_7 & \text{P}_6 & \text{P}_5 & \text{P}_4 & \text{P}_3 & \text{P}_2 & \text{P}_1 & \text{P}_0
\end{array}
\]

\[\text{a}_3\text{a}_2\text{a}_1\text{a}_0 \times 1010 = \text{P}_7\text{P}_6\text{P}_5\text{P}_4\text{P}_3\text{P}_2\text{P}_1\text{P}_0\]

- \(\text{P}_0 = 0\)
- \(\text{P}_1 = \text{a}_0\)
- \(\text{P}_2 = \text{a}_1\)
- \(\text{P}_3 = \text{S}(\text{a}_2 + \text{a}_0)\)
- \(\text{P}_4 = \text{S}(\text{C}(\text{P}_3) + \text{a}_3 + \text{a}_1)\)
- \(\text{P}_5 = \text{S}(\text{C}(\text{P}_4) + \text{a}_2)\)
- \(\text{P}_6 = \text{S}(\text{C}(\text{P}_5) + \text{a}_3)\)
- \(\text{P}_7 = \text{C}(\text{P}_6)\)